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10/606,226	06/26/2003	Hideaki Watanabe	024016-00063	3751

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,226	WATANABE, HIDEAKI	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-12 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-12* is/are allowed.

6)☒ Claim(s) *1,3,5 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is responsive to the amendment filed on 06-19-06. Applicant's arguments with respect to the reference Kokubo et al. (US 5,982,208) have been carefully considered but they are not deemed to be persuasive to overcome the reference. Thus, the claims remain rejected under Kokubo.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation "wherein the counter is a counter for obtaining the **count value** by counting the number of the effective transition edges of the input clock signal, existing during the counting period when the reference clock signal is **only** at a High level" is indefinite because it is misdescriptive. Figure 3 and 4 of the present application show that the counter continuously count regardless the level HIGH or LOW of the reference clock signal. The output clock signal (ST) is continuous throughout the counting cycle. The recitation "when the **count value is changed** from a preceding count value, the frequency of the output clock signal is changed during a period in which the reference clock signal is a Low level, after the **end** of the counting period and before the start of a succeeding counting period" is indefinite because it is misdescriptive. Figure 4 of the present application shows that the counter continuously counts the input clock signal and counting values (1, 2, 3,.. Nv) change continuously during the counting cycle. Count number (Nv) is the count number at the **end** of the counting period and no change in frequency is seen after count (Nv). During a counting period, the period of the reference clock signal, the counter start to count from 1 and the count number is (Nv) at the end of the counting period. After the end of the counting period, the counter is reset and start to count from 1-Nv. (fig. 4 of the present application). Therefore, it is not clear what the recitation "when the count value is changed from **a preceding count value**" is meant by. The Applicant is requested to explain what is the "preceding count value". The recitation " the

counting period" on lines 14-15 dies not have antecedent basis.

Regarding claim 3, the recitation "wherein the counter is a counter for obtaining the count value at the end of each High level period and each Low level period of the reference clock signal" is indefinite because it is misdescriptive. The counter counts the output clock signal (ST) and generates the count value (CN) at any time during the counting period. The count value (CN) is not only obtained at the end of each High level period and each Low level period of the reference clock signal as recited. Note that (CN1) and (CN2) are the total counts of the output signal (ST) during a period of the reference clock. The Applicant is requested to explain what the "count value" is meant by. The recitation "when the count value obtained by counting during a High level period of the reference clock signal is changed from a preceding count value, the frequency of the output clock signal is changed **from** a preceding count value, the frequency of the output clock signal is changed **after** the end of the High level period of the reference clock signal and before the start of the next High level period of the reference clock signal and the characteristics in which when the count value obtained by counting during Low period of the reference clock signal is changed from a preceding count value, the frequency of the output clock signal is changed after the end of the Low level period and before the start of the succeeding Low level period" is confusing. It is not clear what the "a preceding count value" is meant by. Figure 4 of the present shows that during a counting cycle (a low and a high level of the reference clock cycle), the counter counts from 1 to Nv and every count value from 1 to Nv is different. Therefore, every "count value is different from each other during a count cycle. It is not clear what the recitation "when the count value obtained by counting during a High level period of the reference clock signal is changed from a preceding count value, the frequency of the output clock signal is changed from a preceding count value" is meant by.

As understood by the examiner, the counting cycle comprises a Low High level period and a High level period and during a counting cycle the count value changes from 1 to Nv thus; the count values are different from each other during a counting cycle (fig. 4). Clear explanation is required. The recitation "the frequency of the output clock signal changes at the end of the Low level period and before the start of the succeeding Low level period" is indefinite because it is misdescriptive. As understood by the examiner, the frequency of the output clock signal changes at the end of the Low level period and before the start of the succeeding High level period.

Regarding claim 23, there recitation " wherein the counter...when the reference clock

is only at a low level" on lines 13-15 is indefinite because it is misdescriptive. Figures 3, 4 and 5 of the present application shows that the output (ST) of the counter exists when the reference clock (SR) is at both Low and High levels.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 5 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Kokubo et al. (US 5,982,208).

Regarding claim 1, figures 4 and 11 of Kokubo show a clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter (5) for delivering a count value by counting the number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal;

a subtracter (17) for delivering a difference value obtained by subtracting either the count value or a reference value from the other;

a control voltage generation circuit (18, 9, 4) for delivering an analog control voltage (Vr) corresponding to an integrated value of the difference value; and

a voltage control oscillator circuit (1) for delivering the output clock signal (fout) at a frequency corresponding to the analog control voltage;

wherein the counter is a counter for delivering the count value (Nv) by counting the number of the effective transition edges of the output clock signal (fout), existing during the counting period when the reference clock signal (fref) is at a High level.

the counter, the subtracter, the control voltage generation circuit, and the voltage control oscillator circuit (1) having response characteristics such that when the count value (Nv) is changed from a preceding count value, the frequency of the output clock signal is changed during a period in

which the reference clock signal (fref) is a Low level, after the end of the counting period (area 5 of line C) and before the start of a succeeding counting period. Note that the frequency of the output clock signal (fout) changes according to the resulting count value (Nv) (abstract). Figure 4 of Kokubo shows that when the reference clock signal (fref) is at low level and the count value changes from the value [4] to the different value [5] the output frequency also changes because the value of the frequency of the output clock signal (fout) changes with the count value (Nv) (abstract).

Regarding claim 3, figures 4 and 11 of Kokubo show a clock multiplication circuit for delivering an output clock signal (fout) at a frequency that is a multiple of the frequency of a reference clock signal (fref) as inputted, the clock multiplication circuit comprising:

a counter (5) for delivering a count value (Nv) by counting the number of effective transition edges of the output clock signal (fout), existing during a predetermined counting period given on the basis of the reference clock signal;

a subtracter (17) for delivering a difference value obtained by subtracting either the count value (Nv) or a reference value (fref) from the other;

a control voltage generation circuit (18, 9, 4) for delivering an analog control voltage (Vr) corresponding to an integrated value of the difference value; and

a voltage control oscillator circuit (1) for delivering the output clock signal (fout) at a frequency corresponding to the analog control voltage (Vr),

wherein the counter is a counter for obtaining the count value at the end of each High level period and each Low level period of the reference clock signal, and

the counter, the subtracter, the control voltage generation circuit and the voltage control oscillator circuit having response characteristics in which when the count value obtained by counting during a certain High level period of the reference clock signal is changed from a preceding count value, the frequency of the output clock signal is changed from a preceding count value, the frequency of the output clock signal is changed after the end of the High level period of the reference clock signal and before the start of the next High level period of the reference clock signal and the characteristics in which when the count value obtained by counting during a certain Low.

Regarding claim 5, figures 4 and 11 of Kokubo shows a clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter (5) for delivering a count value by counting the number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal;

a subtracter (17) for delivering a difference value obtained by subtracting either the count value or a reference value from the other; a control voltage [generation circuit for delivering an analog control voltage corresponding to an integrated value of the difference value; and

a voltage control oscillator circuit (4, 9, 18) for delivering the output clock signal at a frequency corresponding to the analog control voltage,

wherein the counter delivers the count value after the end of the counting period and in synchronization with the output clock signal (fout), the subtracter generates a difference value in sync with an output clock signal generated after the counter generates a count value in sync with an output clock signal, the control voltage generation circuit generates an analog control signal in sync with an output dock signal generated after the subtracter generates the difference value in sync with the output clock signal.

Regarding claim 23, figures 4 and 11 of Kokubo show a clock multiplication circuit for delivering an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted, the clock multiplication circuit comprising:

a counter (5) for delivering a count value by counting the number of effective transition edges of the output clock signal, existing during a predetermined counting period given on the basis of the reference clock signal;

a subtracter (17) for delivering a difference value obtained by subtracting either the count value or a reference value from the other;

a control voltage generation circuit (4, 9, 18) for delivering an analog control voltage corresponding to an integrated value of the difference value; and

a voltage control oscillator circuit (1) for delivering the output clock signal at a frequency corresponding to the analog control voltage,

wherein the counter is a counter for delivering the count value by counting the number of the effective transition edges of the output clock signal, existing during the counting period when the reference clock signal is at a Low and High levels, and

the counter, the subtracter, the control voltage generation circuit, and the voltage control oscillator circuit having response characteristics such that when the count value is changed from a preceding count value, the frequency of the output clock signal is changed during a period in which the reference clock signal is a High level, after the end of the counting period and before the start of a succeeding counting period. Note that figure 4 of Kokubo shows that at the high level of the reference clock signal (fref) wherein the counts are (Nv-2, Nv-1, Nv), the counts varies from values (Nv-2) to (Nv) before the start of succeeding period, the low level part of the reference clock signal (similar to figure 4 of the present application).

Response to Arguments

In the previous Office Action, the allowance of claim 5 was an error thus; the allowance of claim 5 has been withdrawn. On pages 18-21 of the Remarks, the Applicant argues that "Thus, Kokubo does not disclose or suggest at least the feature of counting the number of effective transition edges of the output clock signal existing during the counting period when the reference clock signal is only at a High level, as in claim 1". This argument is not precise because figures 3 and 4 of the present application show that the counter counts when the reference clock signal is at BOTH HIGH and LOW levels. The counter does not stop counting when the reference clock signal is LOW level. Note that no counter can continuously count an indefinite number and ONLY count when the reference clock is at HIGH level. Depending on the capacity of the counter, when the counting reaches the end, the counter resets and restarts counting as shown in figure 4 of the present application and in figure 4 of Kokubo. Therefore, claims 1 and 3 read on figures 4 and 11 of Kokubo. On page 22, the Applicant argues that claims 6-9 are unrelated to a low-pass filter. Claim 6 recites a "control voltage generation circuit" for delivering an analog control voltage Figure 11 of Kokubo shows a control voltage generation circuit (4, 9,18) for delivering an analog control voltage (Vr) comprising a low-pass filter. A low pass filter is well know to on of ordinary

skill in the art as a device for filtering out unwanted high frequency noise. Therefore the low-pass filter (4) is a necessary part of the control voltage generation circuit (4, 9,18) for generating a good control voltage (Vr). The Applicant argues that Kokubo teaches both the high and low levels as counting period while "claim 23 requires that the counting period exist only when the reference clock signal is at a low level". Figures 3, 4 and 5 of the present application show that the counting period exists when the reference clock signal is at High or Low levels.

Allowable Subject Matter

Claims 6-12 are allowed because the prior art of records (US 5,982,208) fails to teach or suggest a clock multiplication circuit comprising a counter that counts both the rising edge and the falling edge of the clock signal as called for in claim 6; a multiplier for multiplying the difference value by a predetermined factor and delivering a multiplied difference value to the control voltage generation circuit is interposed between the subtracter and the control voltage generation circuit as called for in claim 7; a clock multiplication circuit comprising a subtracter capable of switching the subtracter reference value as called for in claim 11.

Conclusion

Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Hiep Nguyen
08-15-06

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PRIMARY EXAMINER